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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number 10/751,141
Filing Date: December 31, 2003
Appellant(s): FERNANDO GONZALEZ

Robert A. Manware
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01/20/2006 appealing from the Office action mailed 07/14/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20020190344	MICHEJDA ET AL.	12-2002
6271566	TSUCHIAKI	8-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Michejda et al.

Regarding claim 12, Michejda et al. discloses in figure 1A a transistor comprising a drain terminal 178 comprising a doped polysilicon material (para [0034], lines 5-6 and para [0058]) disposed within a first shallow cavity formed in an isolation oxide region 150, 160 (para [0033], lines 4-8); a source terminal 178 comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region; a channel 130 (para [0033], line 3) formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (para [0042]) coupled to each of the drain terminal and the source terminal; and a gate 120 (para [0032], line 2) disposed over the channel and comprising one conductive layer disposed over a gate oxide layer 122 (para [0032], lines 4-5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. in view of Tsuchiaki.

Regarding claim 17, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention (see rejection of claim 12) except a storage device. However, Tschuchiaki teaches storage device connected to a transistor (col. 1,

lines 59-64). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having a storage device connected to a transistor for the purpose of utilizing the improved transistor in a memory cell.

Regarding claim 18, Tsuchiak teaches that the storage device comprises a capacitor (col. 1, lines 59-64).

Regarding claim 22, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention except a memory device coupled to the processor and comprising a storage device. However, Tschuchiaki teaches a memory device coupled to the processor (col.1, lines 42-45) and comprising a storage device (col. 1, lines 59-64). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having a memory device coupled to the processor and comprising a storage device for the purpose of utilizing the improved transistor in an integrated system in a single chip microcomputer.

Claims 13-15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. as applied to claim 12 above.

Regarding claim 13, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify Michejda et al. by having each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 15, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, Michejda et al. discloses in figure 1 substantially all the structure set forth in the claimed invention except each of the first and second conductive posts coupled to the respective drain and source terminals at a distance from the gate being greater than 50% of the width of the respective drain and source terminals. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Michejda et al. by having each of the first and second conductive posts coupled to the respective drain and source terminals at a distance from the gate being greater than 50% of the width of the respective drain and source terminals, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 19-21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michejda et al. and Tsuchiaki as applied to claims 17 and 22 above.

Regarding claims 19 and 23, Michejda et al. and Tsuchiaki disclose substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising a depth in the range of approximately 300A to 1500A, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the

optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 20 and 24, Michejda et al. and Tsuchiaki disclose substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 0.5 to 10, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 21 and 25, Michejda et al. and Tsuchiaki disclose substantially all the structure set forth in the claimed invention except each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Michejda et al. and Tsuchiaki by having each of the plurality of cavities comprising an aspect ratio of less than or equal to approximately 1 to 3, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

(10) Response to Argument

On pages 6-11, with respect to claims 12-17 and 22, Appellant argues in figure 1A of Michejda et al. the isolation oxide structures 150 are formed inside the trenches 140, 145 and the doped polysilicon materials 170 are deposited in the trenches 140, 145 on top of the isolation oxide structures 150, not in an isolation oxide region as recited in claims 12, 17 and 22. Also, in figures 8-18 of Michejda et al. the nitride wall spacers 710, isolation oxide structures 810 and doped polysilicon materials 1010 are each disposed within the trenches 410, 415 formed in the substrate 210. Appellant further states that the "cavity" is used in the present application to distinguish from a trench in which the "trench" refers to the structure formed in the substrate, while the "cavity" refers to the structure formed in the isolation oxide disposed within the trench (page 11, lines 16-20 of the present application). As such, Appellant argues Michejda et al. does not disclose, "cavities formed in an isolation oxide region" and cannot possibly disclose disposing "a doped polysilicon material formed within the cavities formed in the isolation oxide region" as recited in claims 12, 17 and 22. However, as shown in figures 7-18 (showing the process steps of forming the structure of figure 1A) the isolation oxide regions 810, 510 are clearly disposed within the trenches 410, 415 (para [0046], lines 1-8). Hence, the doped polysilicon materials 1010 are formed in the isolation oxide regions 810, 510 within the trenches 410, 415. Therefore, based on the definition of "cavity" of the present application, Michejda et al. discloses the doped polysilicon material is disposed within the shallow cavity formed in an isolation oxide region.

Further, with respect to claims 17 and 22, Tsuchiaki discloses a storage device is connected to a transistor and a memory device coupled to the processor as described in rejection of claims 17 and 22 above. Hence, Tsuchiaki cures the deficiencies of Michejda et al. In other words, the combination of Michejda et al. and Tsuchiaki reads on claims 17 and 22.

Lastly, with respect to claims 13-16, it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working values (or ranges) involves only routine skill in the art. Therefore, it would have been obvious at the time of the present invention to modify Michejda et al. to include the claimed optimum or working values (or ranges) herein.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joseph H. Nguyen

Patent Examiner

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c.c

March 21, 2006.

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